CY590 Datasheet

300M-450MHz ASK Receiver

General Description

CY590 is a single chip from 300MHz to 450MHz frequency range, ASK or OOK RF receiver with wide power supply voltage, low power consumption, high performance, typical 20dB image rejection, typical -110dBm sensitivity and specifically designed without AGC capacitor.

CY590 is a true RF in, data out highly integrated wireless receiver, built-in image rejection mixer and 400 KHz to 600 KHz IF bandwidth BPF. The IF tuning and digital Auto Gain Control (AGC) are accomplished automatically within the device which eliminates external tuning and AGC capacitor, the result is a highly reliable yet low cost solution. The device operates from a wide supply voltage of 2.6V to 5.5V, and typical power consumes 3.5mA of supply current at 315MHz and 4.6mA at 433.92MHz, a shutdown mode reduces supply current to typical 0.8uA, the device supports the date rates up to 5Kbps modulated by typical 1527, 2262 and customized encoding types.

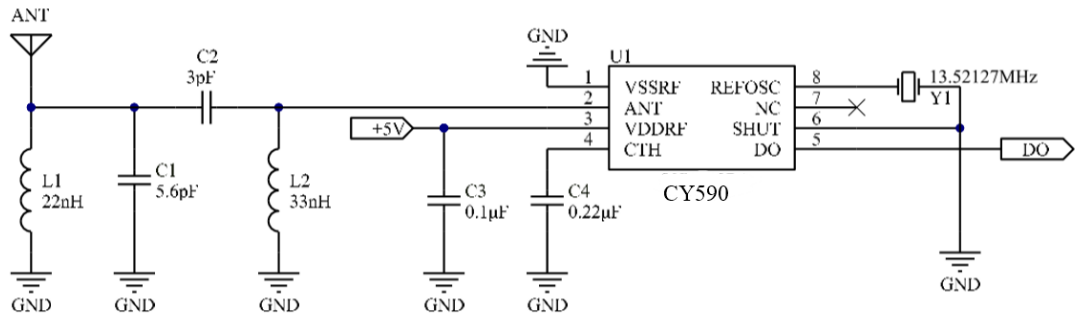
Features

- Frequency Range: 300MHz ~ 450MHz
- Sensitivity: -110dBm (Typical)
- Image Rejection Mixer: 20dBm (Typical)
- IF Bandwidth: 400KHz ~ 600KHz
- Supply Voltage: 2.6V ~ 5.5V
- Low Power Consumption:
  - ✓ 5V Typical 3.5mA (315MHz)
  - ✓ 5V Typical 4.6mA (433.92MHz)
  - ✓ 5V Typical 0.8uA (Shut Down)
- No AGC Capacitor Required
- Data Rates to 5Kbps
- 8-Pin SOP Package

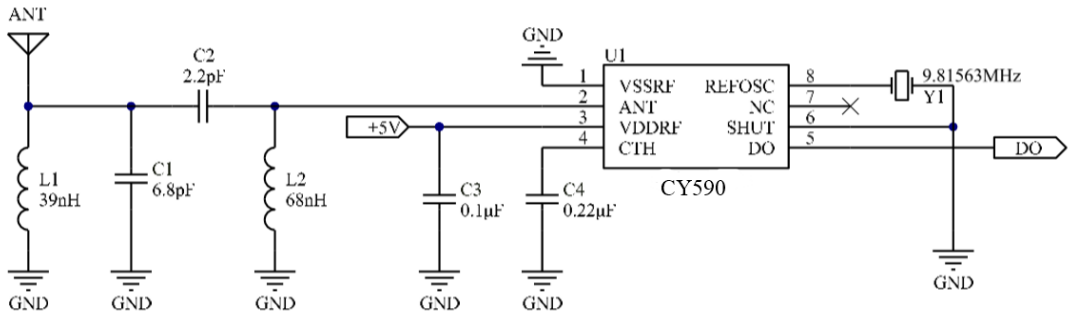
Applications

- Remote Control System
- Remote Keyless Entry (RKE)
- Remote Fan and Light Control
- Home Automation

Typical Application

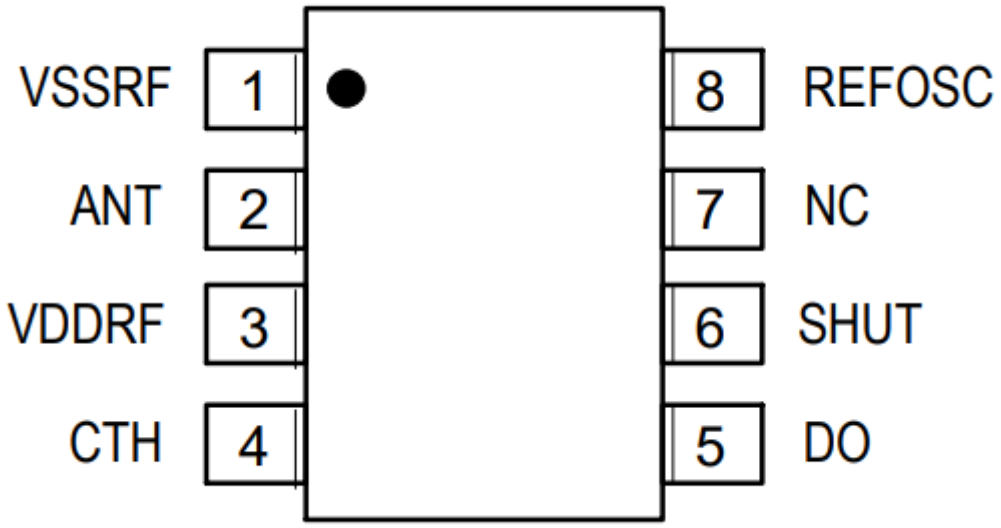


433.92MHz, 1Kbps Application Circuit



315MHz, 1Kbps Application Circuit

Pin Configuration



CY590 8-Pin SOP Package

Pin Description

Pin Number	Pin Name	I/O	Pin Function
1	VSSRF	I	RF Ground Supply.
2	ANT	I	Antenna: the ANT pin should be impedance matched to the antenna.
3	VDDRF	I	RF Power Supply.
4	CTH	IO	Data Slicing Threshold Capacitor.
5	DO	O	Digital Data Output.
6	SHUT	I	Shut Down: Pull “1” to set shut down mode, pull “0” to enable the device.
7	NC	---	No Connection.
8	RFFOSC	I	Reference Crystal Oscillator

Absolute Maximum Ratings

Supply Voltage	6V
Input Voltage	6V
Junction Temperature (T_J)	+150°C
Storage Temperature Range (T_S)	-65°C to +150°C
Lead Temperature (soldering, 10 sec.)	+260°C
ESD Rating	Note 1

Operating Ratings

Supply Voltage	2.6V to 5.5V
Input Voltage (Max.)	5.5V
Ambient Temperature (T_A)	–40°C to +85°C

Electrical Characteristics

Unless otherwise noted, VDD = 5V, CTH = 0.22µF, 1Kbps data rate (Square wave encoded, BER =10E-2), all test at T_A = 25° C.

Receiver

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{RX}	Frequency Input Range		300 to 450			MHz
$P_{IN,MAX}$	Maximum Input Power				10	dBm
P_{SENS}	Receiver Sensitivity (Note 2)	f_{RX} = 315MHz		-110		dBm
		f_{RX} = 433.92MHz		-110		dBm
	Image Rejection	f_{RX} = 315MHz		20		dB
		f_{RX} = 433.92MHz		20		dB
f_{IF}	IF Center Frequency	f_{RX} = 315MHz		0.802		MHz

		f_{RX} = 433.92MHz		1.138		MHz
f_{BW}	IF Bandwidth	f_{RX} = 315MHz		450		kHz
		f_{RX} = 433.92MHz		580		kHz
	Receive Modulation Duty Cycle	Note 3	20		80	%

Reference Oscillator

f_{OSC}	Frequency	f_{RX} = 315MHz	9.81563			MHz
		f_{RX} = 433.92MHz	13.52127			MHz
I_{OSCSC}	Source Current			7.5		uA

DO Drive

	DO pin Output Current	Source @ 0.8VDD		590		uA
		Sink @ 0.2 VDD		850		uA
T_{RISE}	Output Rise and Fall Times	C_L = 15pF, pin DO, 10-90%		1.2		µsec
T_{FALL}				1		µsec

Power Supply

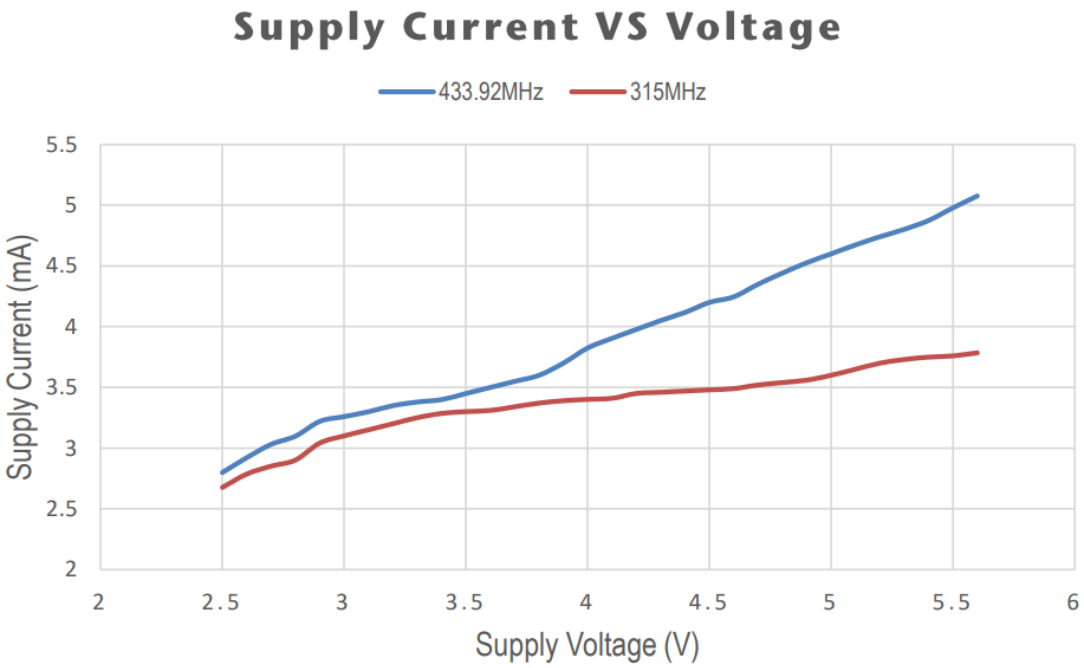
I_{CC}	Supply Current @ VDD = 5V	f_{RX} = 315MHz		3.5		mA
		f_{RX} = 433.92MHz		4.6		mA
I_{OFF}	Shut Down Current	SHUT = High		0.8		µA

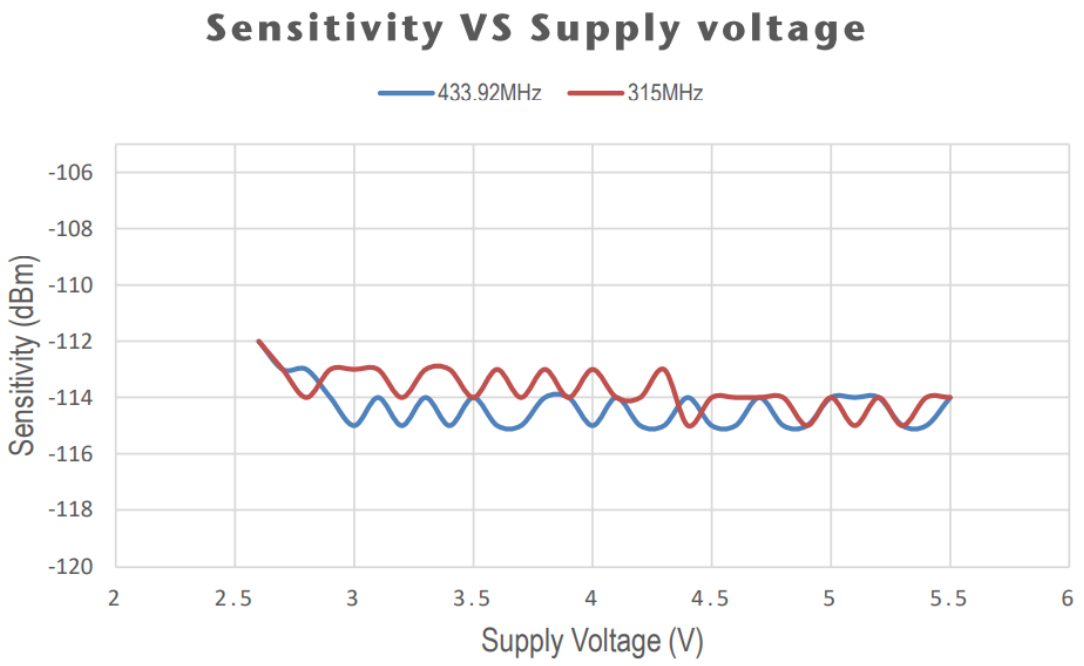
Note 1: Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.

Note 2: Sensitivity is defined as the average signal level measured at the input necessary to achieve 10-2 BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Square wave encoded) at a data rate of 1kbps.

Note 3: When data burst does not contain preamble, duty cycle is defined as total duty cycle, including any “quiet” time between data bursts. When data bursts contain preamble sufficient to charge the slice level on capacitor CTH, then duty cycle is the effective duty cycle of the burst alone.

TYPICAL CHARACTERISTICS





Block Diagram

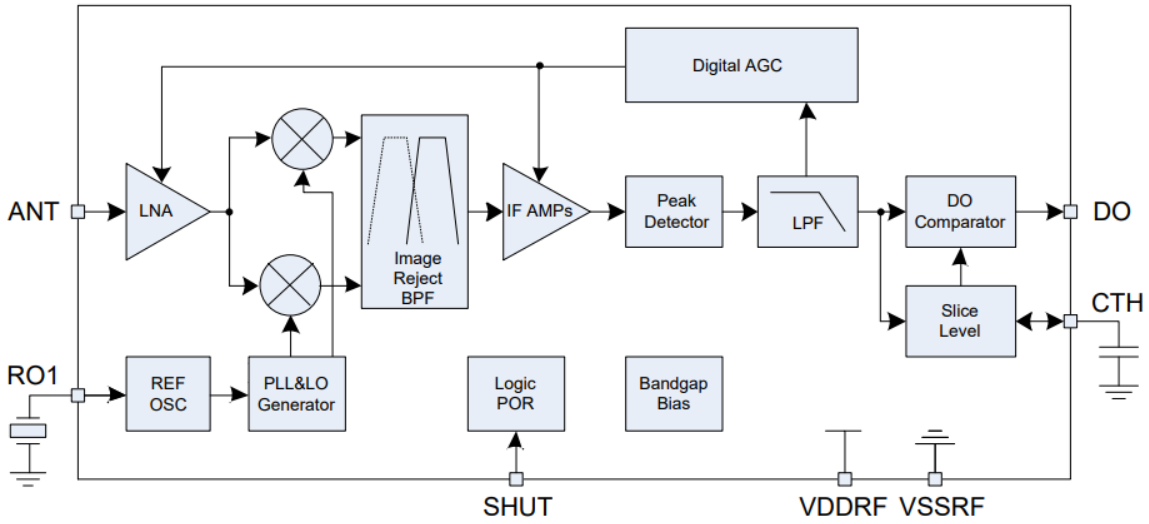


Figure 1. Simplified System Block Diagram

FUNCTIONAL DESCRIPTION

Figure 1 Simplified System Block Diagram that illustrates the basic structure of the CY590. It is composed of several modules; Low Noise Amplifier, Image Rejection Mixer, Band-Pass Filter, IF Amplifiers, Peak Detector, Low-Pass Filter, Digital Auto Gain Control (AGC), DO Comparator, the Slice Level, Reference Oscillator, PLL and LO Generator, Bandgap Bias and Control Logic.

UHF Downconverter

The RF input signal is AC-coupled into the gate circuit of the grounded source LNA input stage. The LNA uses a Cascoded NMOS structure circuit, the LNA outputs are sent to 2 channel mixers and down conversion mixed with the local oscillator signals, and then image rejected and filtering by an image rejection band-pass filter, the signal is converted to IF signal from RF signal after the multistage amplified by IF amplifiers.

OOK Demodulator

The signal prior to DO comparator is still linear demodulated AM. Data comparator converts this signal into digital “1” and “0” by comparing with the threshold voltage built up on the CTH capacitor. After the comparator and output driver, the signal is now digital OOK data.

Digital AGC

The digital AGC monitors the signal amplitude from the output of the LPF, and built-in digital AGC algorithm acts to adjust the gain of the LNA and IF AMPs to compensate for RF input signal level variation.

Reference Oscillator

The reference oscillator in the CY590 uses a basic Colpitts crystal oscillator configuration with MOS transconductor to provide negative resistance. The REFOSC pin external capacitor is integrated inside CY590. User only needs to connect reference oscillation crystal. Reference oscillator crystal frequency can be calculated:

$F_{OSC} = F_{RF}/(32+1.1/12)$.

For 315.00MHz, F_{OSC} = 9.81563MHz;

For 433.92MHz, F_{OSC} = 13.52127MHz.

PACKAGE DESCRIPTION

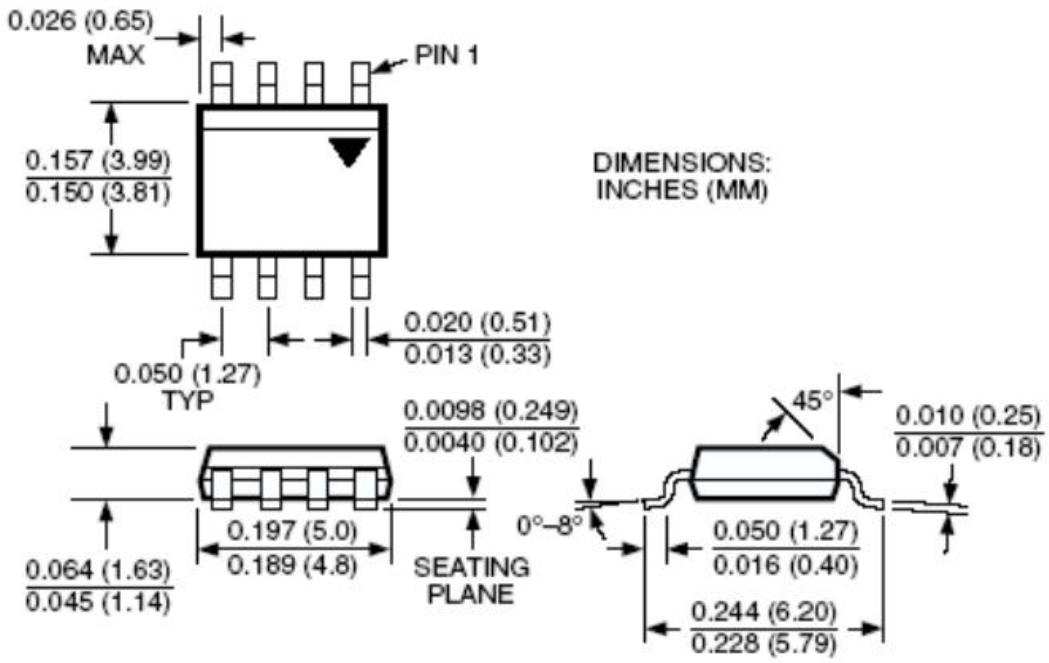


Figure 2 SOP-8 Package Outline Dimension